

EEE361: Digital Design and HDL Modeling

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Objective:

To introduce students to design and modelling small digital circuits in Very High Speed Integrated Circuit Hardware Description Language (VHDL).

By the end of this course students will be able to:

1. Perform Top-Down, Hierarchical analysis.
2. Use VHDL to Model simple hardware component (i.e. ALU, MUX, DFF, Tri-state buffer, etc.).
3. Use VHDL to combine hardware components into a larger circuit (i.e a simple computer).
4. Simulate designs using Active HDL.
5. Synthesize designs to a Spartan 3 Field Programmable Gate Array (FPGA).
6. Calculate Maximum propagation time for combinational logic components in a circuit.
7. Produce a Finite State Machine (FSM), an Algorithmic State Machine (ASM), and/or an Algorithmic State Machine with Data Path (ASMD) from a set of requirements.
8. Translate FSMs and ASMs into VHDL.
9. Analyze an ASMD to determine Control Words to support microprogramming.

Throughout the course students will be exposed to varying levels of design abstraction.

Labs:

You will be developing VHDL models for combinatorial as well as sequential digital circuits. These models will be simulated and synthesised using the *Active HDL* tool.

There will be 6 labs. The first lab will be submitted and marked, but the grade will not be used. Rather this first lab is a “freebie” to learn what your professor requires of you in lab reports. For the other 5 labs, you have to submit a report, which will be graded by your professor.

Submission of labs

- The due-date for submitting your labs will be indicated in the description of each lab/assignment.
- Unless you have permission from your professor to submit your lab late, any late submission is subject to a reduction of your mark.

Quizzes:

There will be a number of short quizzes that will be held during lab periods. The material to be covered by the quizzes is both the content of the course and lab directives. The inclusion of lab directives as material eligible for a quiz is to ensure that students come to lab periods prepared.

Evaluation mode and value:

- Labs 30%
- Quizzes 20%
- Final exam 50%

Policy on Academic Misconduct

Academic misconduct, including plagiarism, cheating, and other violations of academic ethics, is a serious academic infraction for which penalties may range from a recorded caution to expulsion from the College. The RMCC Academic Regulations Section 23 defines plagiarism as: “Using the work of others and attempting to present it as original thought, prose or work. This includes failure to appropriately acknowledge a source, misrepresentation of cited work, and misuse of quotation marks or attribution.” It also includes “the failure to acknowledge that work has been submitted for credit elsewhere.” All students should consult the published statements on Academic Misconduct contained in the *Royal Military College of Canada Undergraduate Calendar*, Section 23.

Schedule:

Classes

Tuesdays	1000 – 1050. Rm S4201
Wednesdays	1000 – 1050. Rm S4201
Thursdays	1200 – 1250. Rm S4202

Lab

Tuesdays	1100 – 1250. Rm S5206
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Required books:

- [1] Zwolinski, *Digital System Design with VHDL*, Prentice Hall, Second Edition, 2004.
- [2] S.Yalamanchili, *Introductory VHDL: From Simulation to Synthesis*, Prentice Hall, 2001.
- [3] M. Morris Mano, and Charles R. Kime, *Logic and Computer Design Fundamentals and Xilinx Student Edition 4.2 Package, 3/E*, Prentice Hall, ISBN: 0-13-124711-5
- [4] Pong P. Chu, *FPGA Prototyping by VHDL Examples: XILINX Spartan-3 Version*, Wiley-Interscience, 2008.

Course’s web-site:

Lectures notes, labs descriptions, and others related information to this course will be available at the following link:

<http://tarpit.rmc.ca>